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L3	33	(cellular adj automata) near20 simulat\$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
Results of search set L1:			
US 20050015688 A1		Phase shifter with reduced linear dependency	20050120 714/700
US 20040255140 A1		Data repository and method for promoting network storage of data	20041216 713/193
US 20040230884 A1		Compressing test responses using a compactor	20041118 714/742
US 20040215922 A1		Efficient addressing method and apparatus for storage	20041028 711/219
US 20040210399 A1		Random number generator method and system for genetic algorithm analysis	20041021 702/20
US 20040172431 A1		Method for synthesizing linear finite state machines	20040902 708/252
US 20040162808 A1		Data repository and method for promoting network storage of data	20040819 707/1
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US 20040153649 A1		Digital authentication with digital and analog documents	20040805 713/176
US 20040143745 A1		Data repository and method for promoting network storage of data	20040722 713/176
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US 20040143725 A1		Knowledge-based methods for genetic network analysis and the whole cell computer system based thereon	20040722 712/28
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US 20040141614 A1		Data encryption apparatus and method	20040722 380/200
US 20040139303 A1		Data repository and method for promoting network storage data	20040715 712/220
US 20040139098 A1		Data repository and method for promoting network storage of data	20040715 707/100
US 20040128599 A1		Decompressor/PRPG for applying pseudo-random and deterministic test patterns	20040701 714/726
US 20040088392 A1		Population mobility generator and simulator	20040506 709/223
US 20040086117 A1		Methods for improving unpredictability of output of pseudo-random number generators	20040506 380/44
US 20040022444 A1		Authentication using a digital watermark	20040205 382/232
US 20030233607 A1		Random pattern weight control by pseudo random bit pattern generator initialization	20031218 714/728
US 20030204541 A1		Seedable pseudo-random number generator	20031030 708/250

US 20030167144 A1	Re-configurable embedded core test protocol for system-on-chips (SOC) and circuit boards	20030904	702/119
US 20030149927 A1	Low hardware overhead scan based 3-weight weighted random BIST architectures	20030807	714/738
US 20030131298 A1	Test pattern compression for an integrated circuit test environment	20030710	714/738
US 20030120988 A1	Continuous application and decompression of test patterns to a circuit-under-test	20030626	714/726
US 20030115521 A1	Method and apparatus for selectively compacting test responses	20030619	714/724
US 20030110193 A1	Method for synthesizing linear finite state machines	20030612	708/252
US 20030097387 A1	Truth table candidate reduction for cellular automata based random number generators	20030522	708/250
US 20030078951 A1	Random number generators implemented with cellular array	20030424	708/250
US 20030076956 A1	Software implementation of cellular automata based random number generators	20030424	380/263
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US 20030032010 A1	Methods of populating data structures for use in evolutionary simulations	20030213	435/6
US 20020169658 A1	System and method for modeling and analyzing strategic business decisions	20021114	705/10
US 20020154769 A1	Method of generating pseudo-random numbers in an electronic device, and a method of encrypting and decrypting electronic data	20021024	380/42
US 20020053057 A1	Test pattern compression for an integrated circuit test environment	20020502	714/738
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US 20020023209 A1	Encryption and decryption of digital messages in packet transmitting networks	20020221	713/160
US 20020016806 A1	Method for synthesizing linear finite state machines	20020207	708/252
US 200200009208 A1	Authentication of physical and electronic media objects using digital watermarks	20020124	382/100
US 20010031050 A1	Key generator	20011018	380/44
US 6845159 B1	Processing method and apparatus for converting information from a first format into a second format	20050118	380/44
US 6829740 B2	Method and apparatus for selectively compacting test responses	20041207	714/729
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US 6205197 B1	Programmable supervisory circuit and applications therefor	20010320	377/16
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US 5914887 A	Congestion based cost factor computing apparatus for integrated circuit physical design automation system	19990622	716/8

US 5903461 A	Method of cell placement for an integrated circuit chip comprising chaotic placement and moving windows	1990511	700/121
US 5875117 A	Simultaneous placement and routing (SPAR) method for integrated circuit physical design automation system	1990223	716/14
US 5870313 A	Optimization processing for integrated circuit physical design automation system using parallel moving windows	1990209	716/10
US 5841947 A	Computer implemented machine learning method and system	19981124	706/13
US 5815403 A	Fail-safe distributive processing method for producing a highest fitness cell placement for an integrated circuit chip	19980929	716/9
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US 5781439 A	Method for producing integrated circuit chip having optimized cell placement	19980714	700/121
US 5761077 A	Graph partitioning engine based on programmable gate arrays	19980602	716/7
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US 5724425 A	Method and apparatus for enhancing software security and distributing software	19980303	705/52
US 5682322 A	Optimization processing for integrated circuit physical design automation system using chaotic fitness improvement method	19971028	716/2
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US 5495419 A	Integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing	19960227	700/121
US 5475694 A	Fuzzy multiple signature compaction scheme for built-in self-testing of large scale digital integrated circuits	19951212	714/732
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US 5394405 A	Universal weight generator	19950228	714/739
US 5390282 A	Process for problem solving using spontaneously emergent self-replicating and self-improving entities	19950214	706/13

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US 5043988 A	Method and apparatus for high precision weighted random pattern generation	19910827	714/739
US 4961159 A	Cellular automaton for generating random data	19901002	708/250
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US 4809202 A	Method and apparatus for simulating systems described by partial differential equations	19890228	703/9
US 4691291 A	Random sequence generators	19870901	708/250
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US 20040210399 A	Electronic chromosomes population memory initializing method, involves generating random number sequence by cellular automata for use in population memory of electronic chromosomes	20041021	
US 20030097387 A	Search space reduction method for viable cellular automata based random number generator, involves accepting/rejecting number of random number generators, based on counting number of zero's and one's in truth table	20030522	
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US 20030076956 A	Cellular automata based random generator emulating method, involves automatically generating software emulator and outputting results of simulation step	20030424	
KR 2002004022 A	Method and apparatus for generating random numbers using multi-dimensional cellular automata	20020116	
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1 [Applications of reconfigurable computing: A reconfigurable FPGA-based readback signal generator for hard-drive read channel simulator](#)

Jinghuan Chen, Jaekyun Moon, Kia Bazargan

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: [pdf\(189.66 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A hard disk readback signal generator designed to provide noise-corrupted signals to a channel simulator has been implemented on a Xilinx Virtex textrmTME FPGA device. The generator simulates pulses sensed by read heads in hard drives. All major distortion and noise processes, such as intersymbol interference, transition noise, electronics noise, head and media nonlinearity, intertrack interference, and write timing error, can be generated according to the statistics and parameters de ...

2 [Random numbers for simulation](#)



Pierre L'Ecuyer



October 1990 **Communications of the ACM**, Volume 33 Issue 10



Full text available: [pdf\(2.82 MB\)](#)



Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

In the mind of the average computer user, the problem of generating uniform variates by computer has been solved long ago. After all, every computer :system offers one or more function(s) to do so. Many software products, like compilers, spreadsheets, statistical or numerical packages, etc. also offer their own. These functions supposedly return numbers that could be used, for all practical purposes, as if they were the values taken by independent random variables, with a uniform distributi ...

- 3 Techniques for empirical testing of parallel random number generators 
Paul D. Coddington, Sung-Hoon Ko
July 1998 **Proceedings of the 12th international conference on Supercomputing**
Full text available:  [pdf\(959.36 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)



- 4 A cellular automata simulation system: version 2.0 
J. Dana Eckart
August 1992 **ACM SIGPLAN Notices**, Volume 27 Issue 8
Full text available:  [pdf\(449.03 KB\)](#) Additional Information: [full citation](#), [index terms](#)

- 5 Progress in Picture Processing: 1969--71 
Azriel Rosenfeld
June 1973 **ACM Computing Surveys (CSUR)**, Volume 5 Issue 2
Full text available:  [pdf\(2.34 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

- 6 VLSI Circuits: Selective-run built-in self-test using an embedded processor 
Sungbae Hwang, Jacob A. Abraham
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**
Full text available:  [pdf\(181.75 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Many systems-on-a-chip (SOCs) include processors as central units to implement diverse algorithms and control peripheral units such as embedded cores. The computing power of the embedded processor can be used to self-test its own functions as well as to test the other cores within the chip boundary. In BIST methodology, pseudo-random pattern testing can reduce the memory requirements. In addition to general pseudo-random pattern testing, this paper proposes and evaluates a novel selective-random ...

Keywords: SOC testing, built-in self-test, design for testability, processor-based testing, pseudo-random number generator

- 7 Evolutionary computing and optimization: Co-evolving an effective fitness sample: experiments in symbolic regression and distributed robot control 
Brad Dolin, Forrest H Bennett, Eleanor G. Rieffel
March 2002 **Proceedings of the 2002 ACM symposium on Applied computing**
Full text available:  [pdf\(573.90 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We investigate two techniques for co-evolving and sampling from a population of fitness cases, and compare these with a random sampling technique. We design three symbolic regression problems on which to test these techniques, and also measure their relative performance on a modular robot control problem. The

methods have varying relative performance, but in all of our experiments, at least one of the co-evolutionary methods outperforms the random sampling method by guiding evolution, with subst ...

Keywords: co-evolution, distributed control, fitness cases, genetic algorithms, genetic programming, robot control, symbolic regression

8 Programmable applications: interpreter meets interface

Michael Eisenberg

April 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 2


Full text available:  [pdf\(4.42 MB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

Current fashion in "user-friendly" software design tends to place an over-reliance on direct manipulation interfaces. To be truly expressive (and thus truly user-friendly), applications need both learnable interfaces and domain-enriched languages that are accessible to the user. This paper discusses some of the design issues that arise in the creation of such *programmable applications*. As an example, we present "SchemePaint," a graphics application that combines a MacPaint-like interface ...

9 The use of cellular automata in the classroom

H. Albert Lilly

December 1995 **Proceedings of the 1995 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available:  [html\(28.99 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

10 Modeling the software architecture of a prototype parallel machine

M. Ajmone Marsan, G. Balbo, G. Chiola, G. Conte

May 1987 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1987 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 15 Issue 1

Full text available:  [pdf\(1.17 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A high-level Petri net model of the software architecture of an experimental MIMD multiprocessor system for Artificial Intelligence applications is derived by direct translation of the code corresponding to the assumed workload. Hardware architectural constraints are then easily added, and formal reduction rules are used to simplify the model, which is then further approximated to obtain a performance model of the system based on generalized stochastic Petri nets. From the latter model it i ...

11 BIST hardware generator for mixed test scheme

C. Dufaza, H. Viallon, C. Chevalier

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available:  [pdf\(831.33](#)

[KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [citations](#)

Deterministic testing is by far the most interesting Built-in Self-Test (BIST) technique due to the minimal number of test patterns it requires and to its predefined fault coverage. However, such a technique is not applicable since despite their efficiency the existing deterministic test pattern generators are enormous consumers of overhead silicon area. Therefore, we propose a mixed test scheme which consists in applying to the circuit under test, a pseudo-random test sequence followed by a det ...


Keywords: ATPG tool, BIST hardware generator, VLSI, automatic testing, binary sequences, built-in self test, deterministic test sequence, digital integrated circuits, integrated circuit testing, logic testing, maximal fault coverage detection, mixed test scheme, pseudo-random test sequence, silicon area overhead

12 Von Neumann hybrid cellular automata for generating deterministic test sequences



D. Kagaris, S. Tragoudas

July 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 3

Full text available:  [pdf\(143.85 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We propose an on-chip test pattern generator that uses an one-dimensional cellular automaton (CA) to generate either a precomputed sequence of test patterns or pairs of test patterns for path delay faults. To our knowledge, this is the first approach that guarantees successful on-chip generation of a given test pattern sequence (or a given test set for path delay faults) using a finite number of CA cells. Given a pair of columns (Cu, C


Keywords: built-in self-test (BIST), cellular automata, test pattern generation

13 Architectures: A perspective on the future of massively parallel computing: fine-grain vs. coarse-grain parallel models comparison & contrast



Predrag T. Tasic

April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available:  [pdf\(277.49 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Models, architectures and languages for *parallel computation* have been of utmost research interest in computer science and engineering for several decades. A great variety of parallel computation models has been proposed and studied, and different parallel and distributed architectures designed as some possible ways of harnessing parallelism and improving performance of the general purpose computers. *Massively parallel connectionist models* such as *artificial neural networks* (...


Keywords: cellular automata, distributed systems, massively parallel computing, multiprocessor computers, neural networks, parallel computation models

14 Adaptation/load balancing: Resource-aware exploration of the emergent dynamics of simulated systems



Sven A. Brueckner, H. Van Dyke Parunak

July 2003 **Proceedings of the second international joint conference on Autonomous agents and multiagent systems**

Full text available:  [pdf\(261.47 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The emerging science of simulation enables us to explore the dynamics of large and complex systems even if a formal representation and analysis of the system is intractable and a construction of a real-world instantiation for the purpose of experimentation is too expensive. A computer simulation model can be run for many more configurations and the accumulated observations deepen our understanding of the system's operation, but it is very important that we have tools that help us manage the huge ...

Keywords: graph coloring, multi-agent coordination, phase change, search, simulation, system dynamics, tools and methods

15 Introduction & overview of "artificial life"—evolving intelligent agents for modeling & simulation



A. Martin Wildberger

November 1996 **Proceedings of the 28th conference on Winter simulation**


Full text available:  [pdf\(987.66 KB\)](#) Additional Information: [full citation](#), [references](#)

16 Reliable computation with cellular automata



Péter Gács

December 1983 **Proceedings of the fifteenth annual ACM symposium on Theory of computing**

Full text available:  [pdf\(809.17 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


We construct a one-dimensional array of cellular automata on which arbitrarily large computations can be implemented reliably, even though each automaton at each step makes an error with some constant probability. To compute reliably with unreliable components, von Neumann proposed Boolean circuits whose intricate interconnection pattern (arising from the error-correcting organization) he had to assume to be immune to errors. In a uniform cellular medium, the error-correcting organization e ...

17 Hardcoding finite state automata processing



E. Ketcha Ngassam, Bruce W. Watson, Derrick G. Kourie

September 2003 **Proceedings of the 2003 annual research conference of the South African institute of computer scientists and information technologists on Enablement through technology**

Full text available:  [pdf\(206.66 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

To hardcode and algorithm means to build into it the data that it requires. In this paper, we present various experiments in hardcoding the transition table of a finite state machine directly into string-recognizing code. Experiments are carried out in two phases. The first phase is limited to the analysis of the hardcoded behavior in relation to acceptance or rejection of a single symbol in some arbitrary state of some finite automaton. Then follows a simulation of the analysis of some hardcoded ...

Keywords: algorithms, automata, experimentation, hardcoding, pattern matching, performance

18 What have we learnt from using real parallel machines to solve real problems?

G. C. Fox

January 1989 **Proceedings of the third conference on Hypercube concurrent computers and applications - Volume 2**



Full text available:  [pdf\(4.08 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We briefly review some key scientific and parallel processing issues in a selection of some 84 existing applications of parallel machines. We include the MIMD hypercube transputer array, BBN Butterfly, and the SIMD ICL DAP, Goodyear MPP and Connection Machine from Thinking Machines. We use a space-time analogy to classify problems and show how a division into synchronous, loosely synchronous and asynchronous problems is helpful. This classifies problems into those suitable for SIMD or MIMD ...

19 Multiplicative Window Generators of Pseudo-random Test Vectors

Janusz Rajske, Jerzy Tyszer

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Full text available:  [pdf\(808.72 KB\)](#)  [Publisher Site](#) Additional Information: [full citation](#), [abstract](#)

New arithmetic two-dimensional generators of pseudo-random test vectors are presented. As an integral part of a recently proposed arithmetic built-in self test (ABIST) environment, all generation functions are executed by basic building blocks performing regular functions of data path architectures, yet the scheme is compatible with scan, parallel scan, partial scan and boundary scan designs. The need for extra hardware is either entirely eliminated or drastically reduced, test vectors can be ea ...

Keywords: Accumulators, Arithmetic generators, Built-in self test, Data-path architectures, Pseudo-exhaustive generators, State coverage

20 Models and languages for parallel computation

David B. Skillicorn, Domenico Talia

June 1998 **ACM Computing Surveys (CSUR)**, Volume 30 Issue 2

Full text available:  [pdf\(298.05 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We survey parallel programming models and languages using six criteria to assess their suitability for realistic portable parallel programming. We argue that an ideal model should be easy to program, should have a software development methodology, should be architecture-independent, should be easy to understand, should guarantee performance, and should provide accurate information about the cost of programs. These criteria reflect our belief that developments in parallelism must be driven by ...

Keywords: general-purpose parallel computation, logic programming languages, object-oriented languages, parallel programming languages, parallel programming models, software development methods, taxonomy

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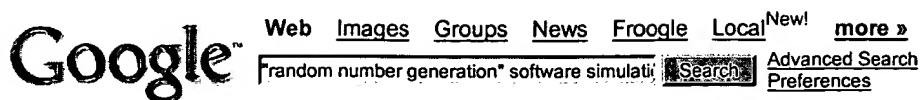
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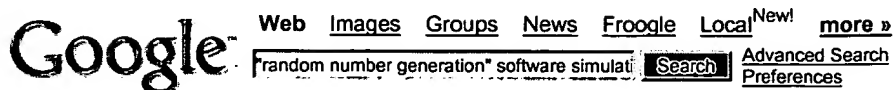
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